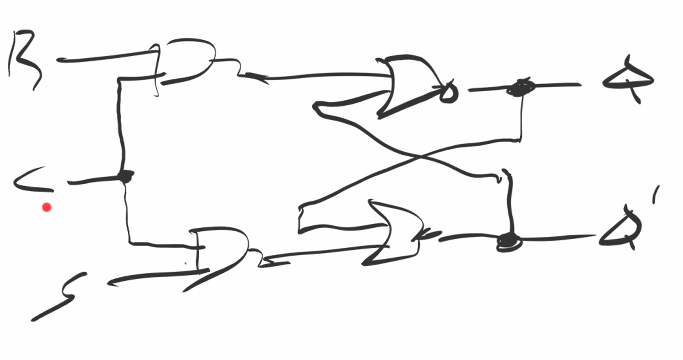
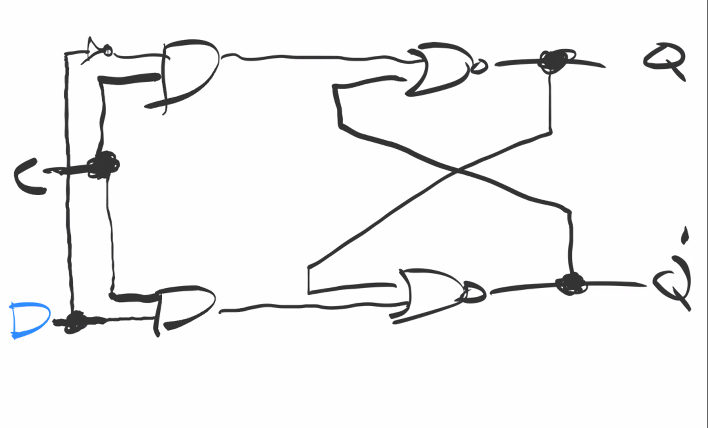
**LECTURE 8**



**R and S can’t be high at the same time. As the latch can go to an undesirable condition.**

**So, to overcome that condition following changes can be made: -**

**D-Latch (Data Latch): - It can store one bit of data.**



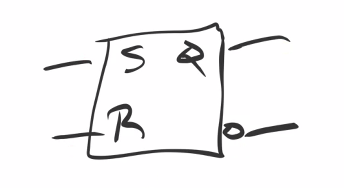
**C D Qnext**

**0 x no change**

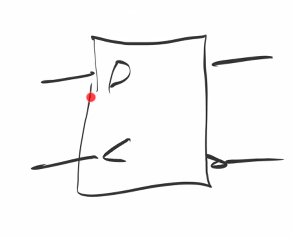
**1 0 0**

**1 1 1**

**SR-Latch**



**D-Latch**

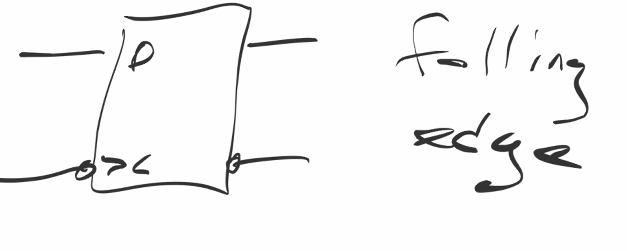


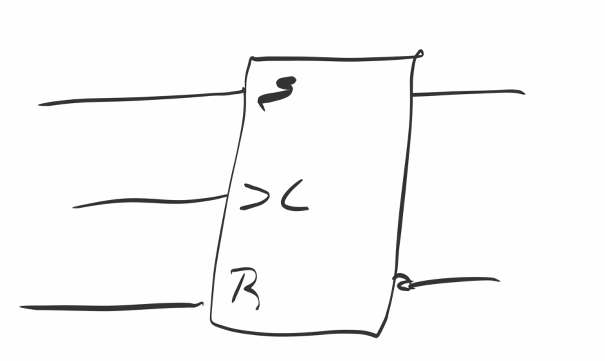
**Both of these latches are level edge triggered**

**D-Latch edge triggered on rising edge:-**



**D-Latch edge triggered on Falling edge:-**

**Edge Triggered Rising Edge:-**



**Flip Flops is a circuit with two stable states.**

**D Flip-Flop(data)**

**JK Flip Flop (Set, Rest, compliment)**

**T Flip Flop (Toggle)(toggle means compliment)**

**JK Flip Flop**

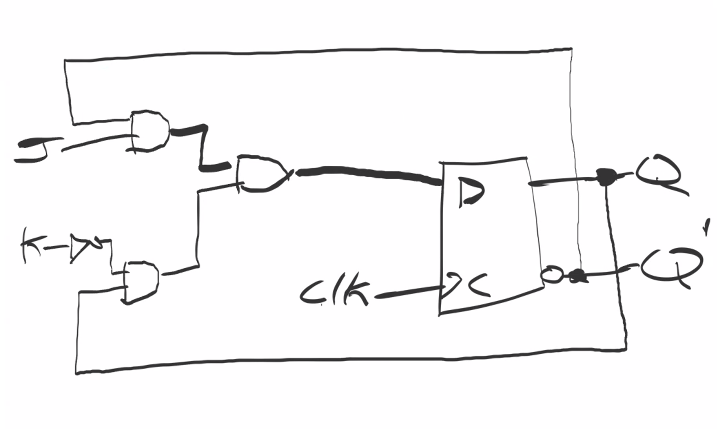
**J K output**

**0 0 no change**

**0 1 reset**

**1 0 set**

**1 1 complement**



**Output depends on the state of the circuit and also JK.**

**J K Qnext**

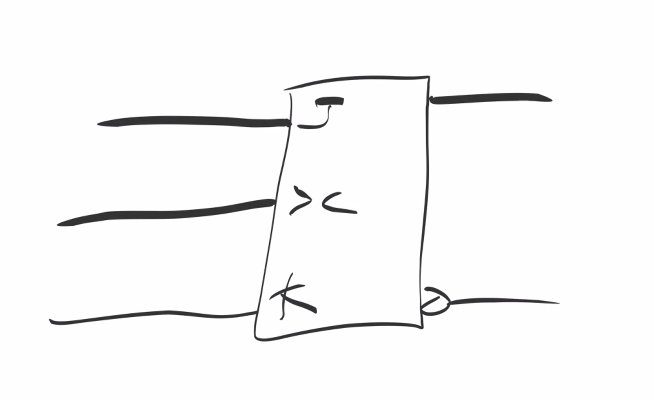
**0 0 Q**

**0 1 0**

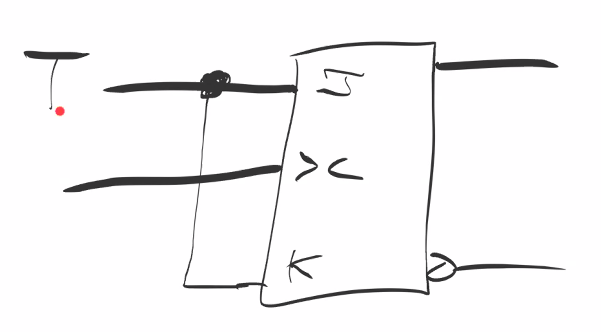
**1 0 1**

**1 1 Q’**

**D=JQ’+K’Q**



**T-Flip Flops(using JK Flip Flops)**

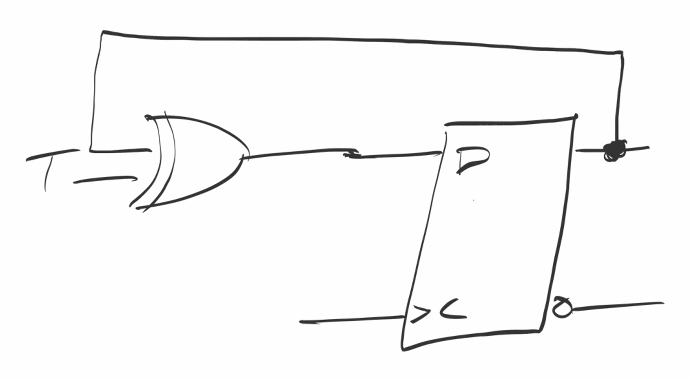


**T Q**

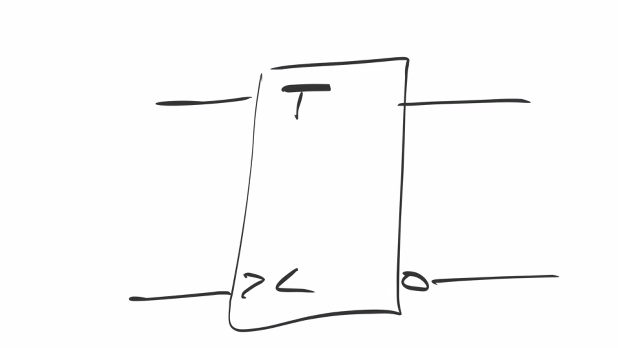
**0 Q**

**1 Q’**

**T-flip flop using D Latch**



**Symbol for T-Flip Flop**



* **Flip Flop char EQ**

1. **Q(t+1) =D**

**JK Q(t+1) =JQ’+K’Q**

**T Q(t+1) =TQ’+TQ**

**Three Bit Register:-**

